Attorney's Docket No.: 042390.P4537

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	Examiner: Wells, Kenneth B.
Melik Isbara	Art Group: 2816
Serial No.: 08/925,868	
Filed: September 9, 1997	
For: **METHOD AND APPARATUS FOR INTERFACING MIXED VOLTAGE SIGNALS**	

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Mail Stop Amendment
Commissioner for Patents
Post Office Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Melik Isbara, hereby declare that:

1. I am a citizen of the United States.

2. I currently reside at 2617 NE Nova Avenue, Hillsboro, Oregon 97124.

3. I am currently an employee at Intel Corporation ("Intel") in Hillsboro, Oregon.

4. I have been employed by Intel from 1992 to present.

5. My current title at Intel is Technical Project/Program Manager.

5. My current title at Intel is Technical Project/Program Manager.

6. I am the inventor for the above-identified patent application.

7. I have assigned all rights in the above-identified patent application to Intel Corporation.

8. I have reviewed the article by David Greenhill, et al., "FA 10.2: A 330MHz 4-Way Superscalar Microprocessor", Digest of Technical Papers, ISSCC97/February 1997 – Session 10, IEEE International Solid-State Circuits Conference, pages 166-167, conference dates February 6-8, 1997 ("Greenhill"). The Examiner has cited Greenhill against the claims of the above-identified application.

9. The invention disclosed and claimed in the above-identified patent application (also referred to here as "my buffer design") was conceived in the United States of America at least as early as May 1996 as evidenced by the document "Modified Input Buffer Design/Characterization Review" (Exhibit "A"). This document was reduced to writing internally within Intel at least as early as the date on the document, *i.e.*, May 1996. This document shows simulation results for may buffer design; see for example the circuit schematic of an input buffer on page 5, and the explanatory text referring to PMOS Pr and PMOS Pcap. This document was prepared under my direction based on my own original work. Between May 1996 and February 1997, I gave high priority to directing simulations and testing of integrated circuits containing my buffer design, as well as preparing Invention Disclosure No. 6384, dated February 20, 1997 (Exhibit "B").

10. In October 1996, I attended an input buffer selection meeting whose minutes in the form of an email are enclosed (Exhibit "C"). This email states that using a broad set of evaluation criteria applied to the simulation results (very detailed simulations including layout extracted parasitics and the package models), my input buffer design named "inmis" overall performs better than the other candidates intended to be included in a test chip (named AQS) and a subsequent product. The other

candidates were used on previous products, thus their simulation based performance were correlated to real measurements. The fact that inmis performed overall better than the other candidates using the same simulation assumptions/tools/techniques, it was expected that its performance on the test chip or the product would be as good as simulations showed. The integrated circuit containing my buffer design (CPU chip code named P55C AQS) was to be actually built sometime later and then tested in February 1997.

11. It is well established that simulation tools are very accurate and the results are closely correlated to real measurements within a few percentage points. Therefore, any actual circuit testing of my input buffer design in P55C AQS would have confirmed the behavior of my buffer design as reported in the simulations referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon.

Respectfully submitted,

Dated: August 9, 2004

Melik Isbara

Full Name : Melik Isbara
Citizenship : U.S.A.
Residence : 2617 NE Nova Avenue
Hillsboro, Oregon 97124

Modified Input Buffer Design/Characterization Review

Melik Isbara, Jason Mo

May, 1996

Agenda

- Circuit Design
- Characterization Data

Target

- Design targets:
  - 2.5V input, 1.8V core
  - delay = 0.7ns @ TTTT, 110C, 1.45V, 0.5pF, 1V/ns, ESD and package model included
  - 2.3V max. gate oxide stress
  - Buffer functional under SSSS, low temperature & low VCC corner.
  - pass-gate +AC coupling capacitor input buffer topology

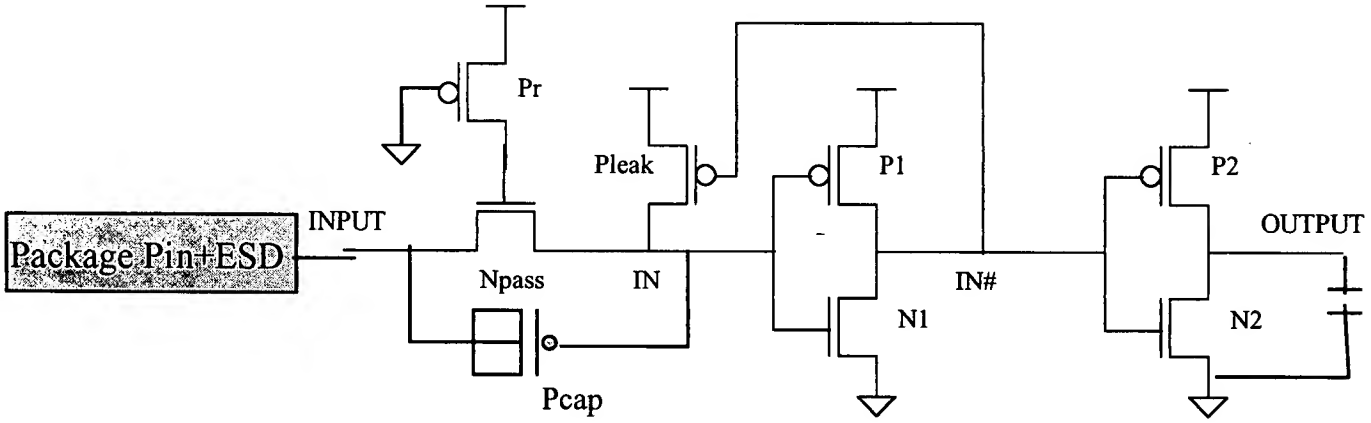
Simulation Setup:

- Process File: P856_x4v2.upf
  - —New process file with higher Vt value.
- Input Waveform:
  - —0-2.5v piecewise linear input.

    T(0-20%)=T(20%-80%)=T(80%-100%)

  - —0.7v-1.7v linear input (since Vil_max=0.7v, Vih_min=1.7v).

Input Buffer



- PMOS Pr provides bootstrapping effect and ESD protection
- PMOS Pcap provides AC coupling between input and node in, so the transient delay between these two nodes is decreased.

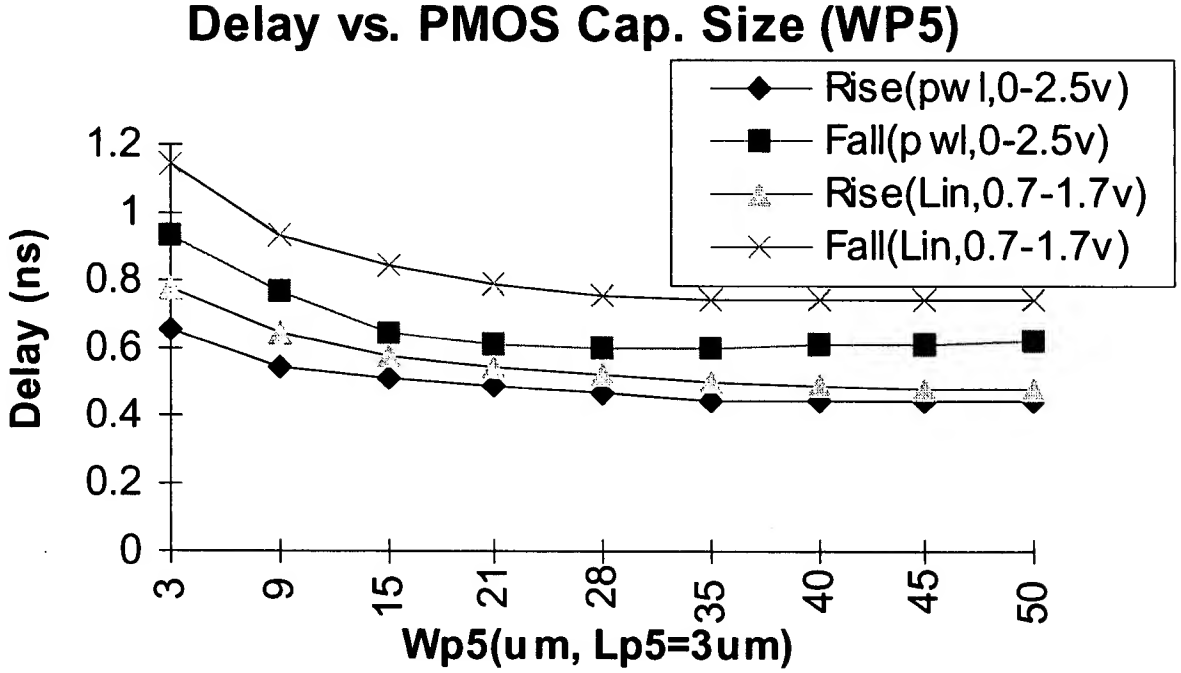
Circuit Design

- Delay: TTTT, 1.45V, 110C, 0.5pF, 1V/ns
  - ***L=0.48μ*** for pass-gate and inverters
  - With 0-2.5v piecewise linear input
    - rising edge delay = 0.47 ns
    - falling edge delay = 0.60 ns
  - With 0.7-1.7v linear input
    - rising edge delay = 0.52 ns
    - falling edge delay = 0.76 ns

Circuit Design

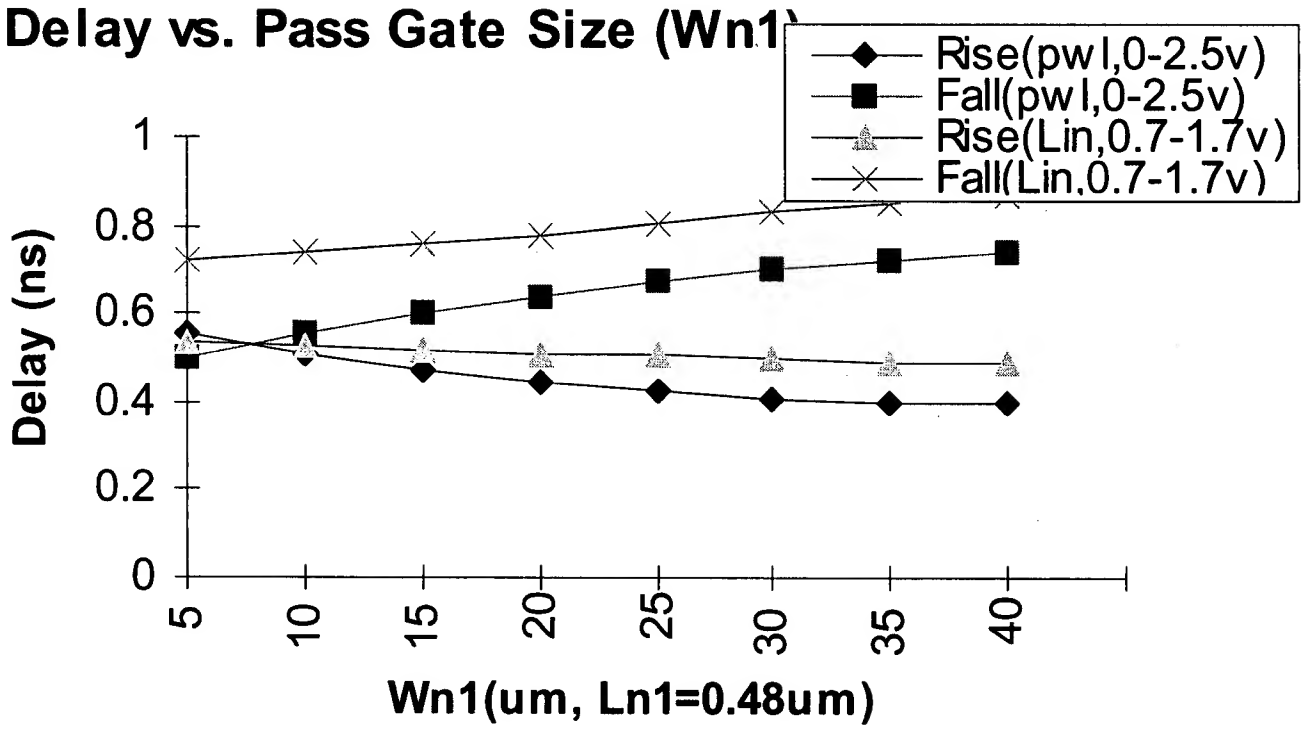
- Sizes:
  - Pr = 2/0.6 P_leak = 0.6/2 Pcap=28/3
  - N_pass= 15/0.48
  - P1 = 39/0.48 N1 = 3/0.48
  - P2 = 16/0.4 N2 = 25/0.4
  - if P1/N1 < 13/1 ratio, buffer can t pass 300mv VCC noise @TTTT, -10C, 0.05pF.

Circuit Design



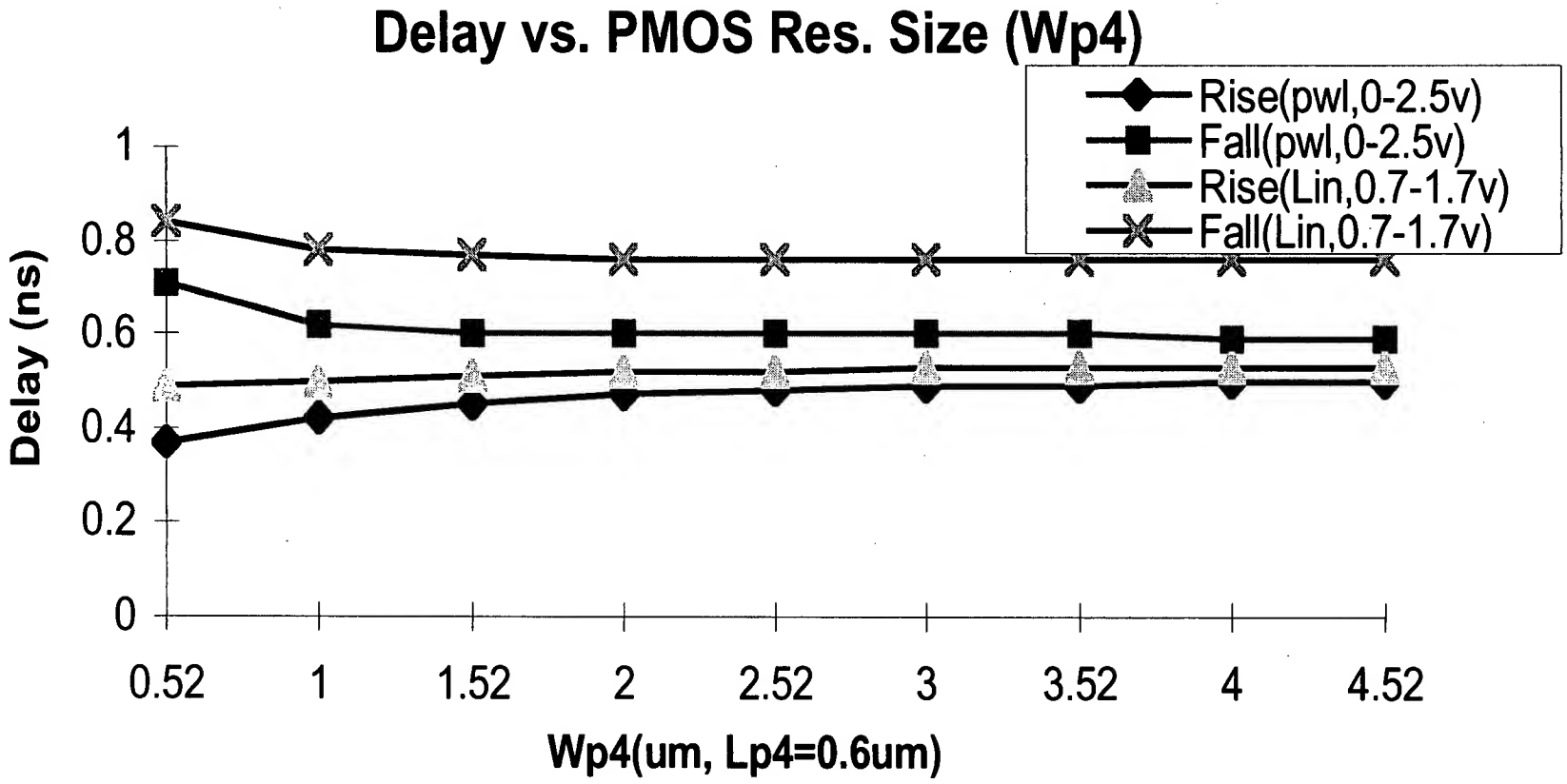
- @ TTTT, 1.45V, 110C, 0.5pF

Circuit Design



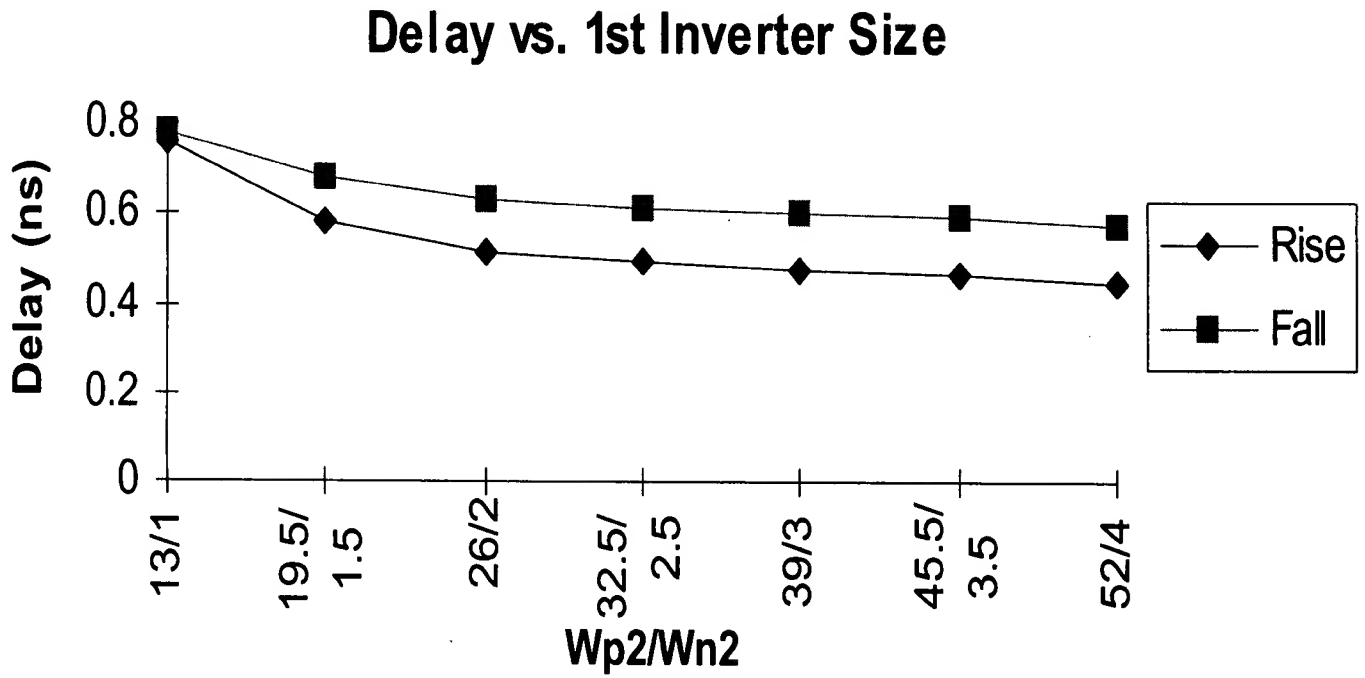
- @ TTTT, 110C, 1.45V, 0.5pF

Circuit Design



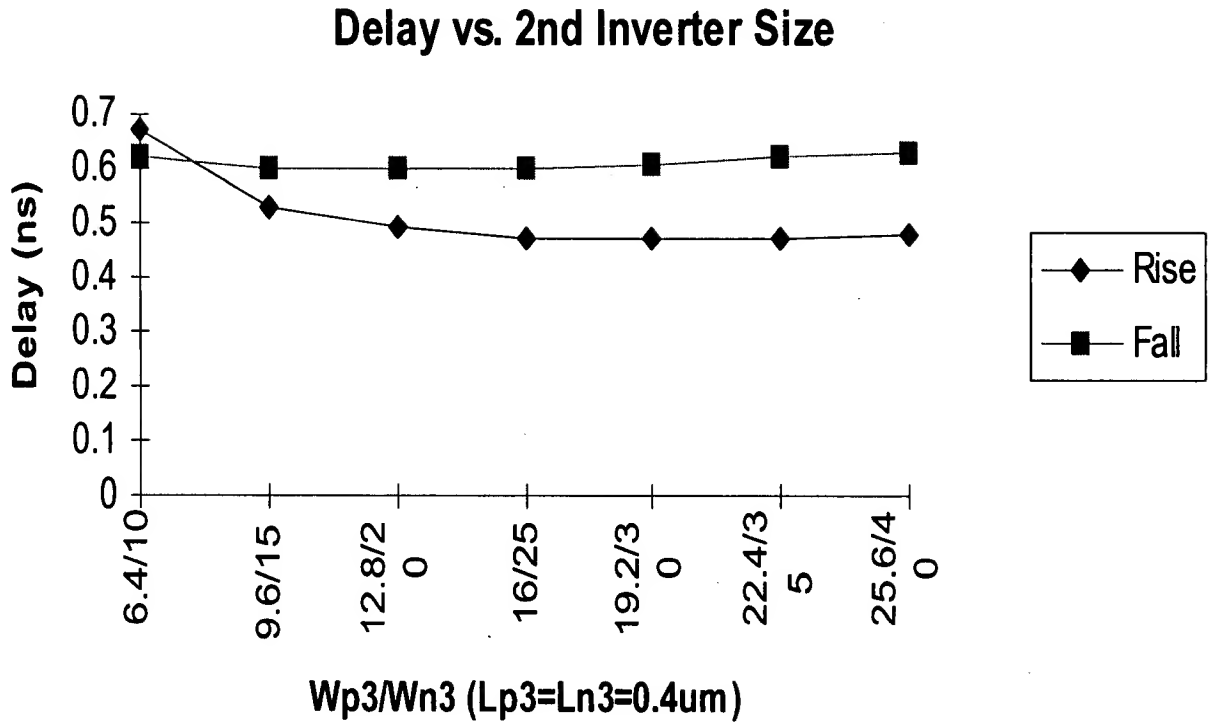
- @TTTT, 110C, 1.45V, 0.5pF

Circuit Design



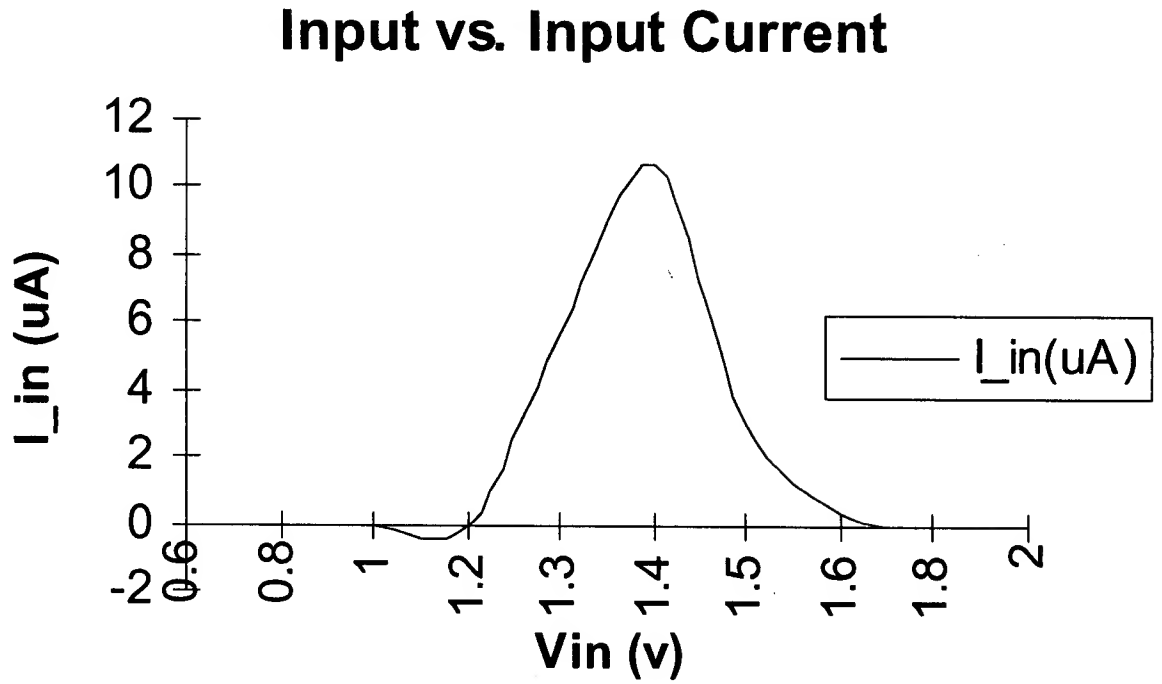
- @TTTT, 110C, 1.45V, 0.5pF
- Pass +/- 300mv power supply noise @ TTTT, 0.05pF, -10C.

Circuit Design



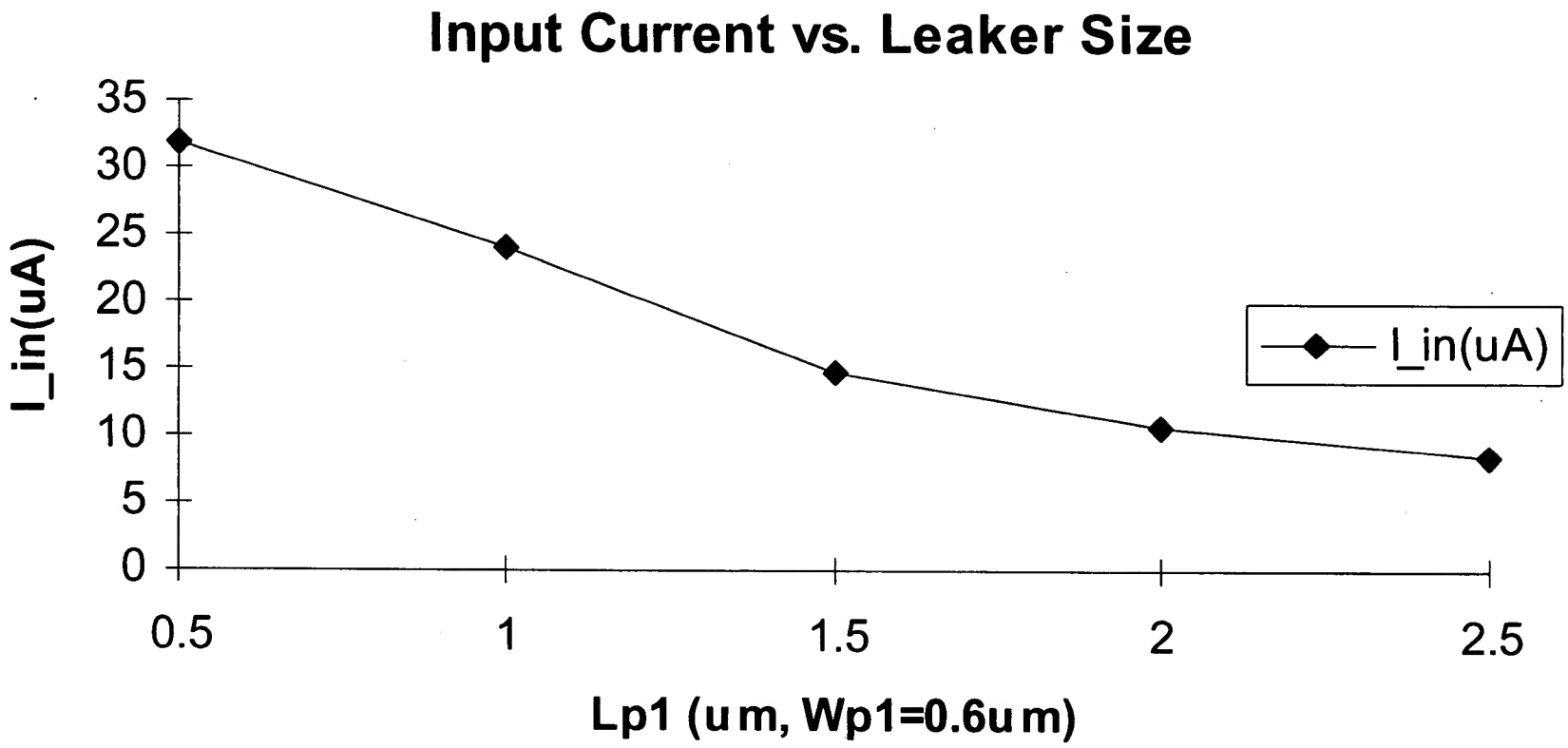
- @TTTT, 110C, 1.45v, 0.5pF
- These sizes give equal HL& LH delay of 0.49ns @TTTT, 50C, 1.8v, 0.5pF

Circuit Design



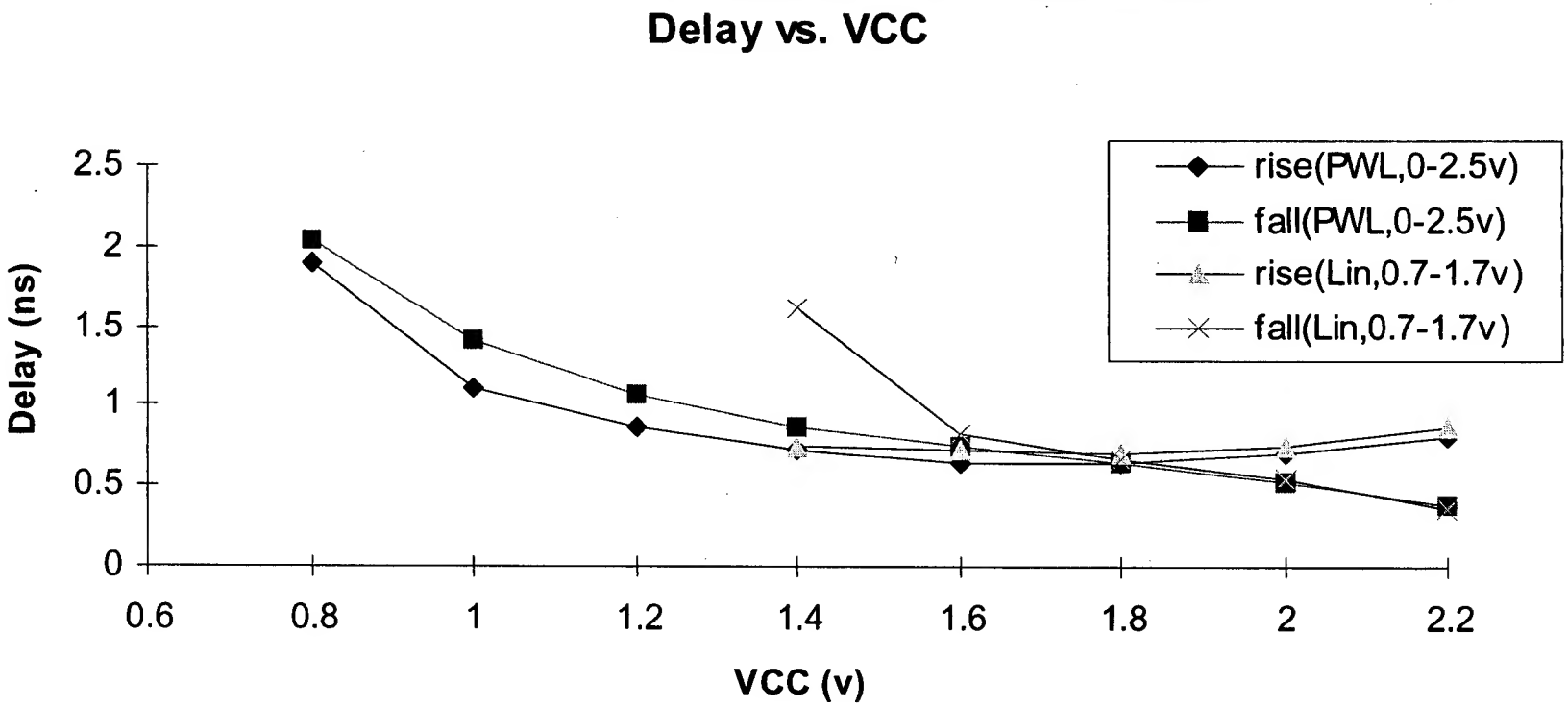
- @FFFF, -5C, 2.05v, 0.5pF
- Used Wp1=0.6um, Lp1=2um. Input current is maximum when Vin=1.4v.

Circuit Design



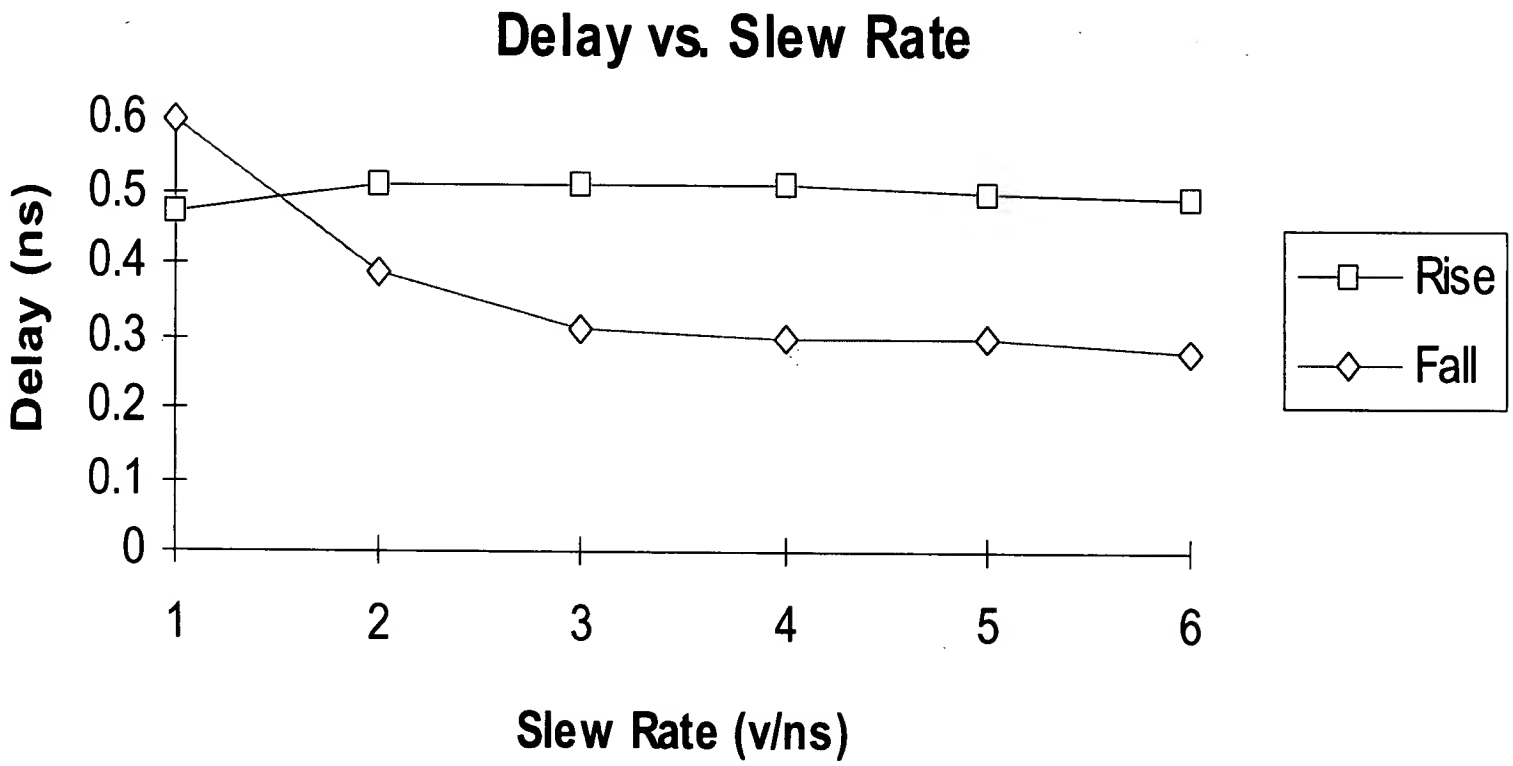
- @FFFF, -5C, 2.05v, 0.5pF, Vin=1.4v
- Final Size: Wp1=0.6um, Lp1=2um, => Iin=11uA.

Delay Characterization Data



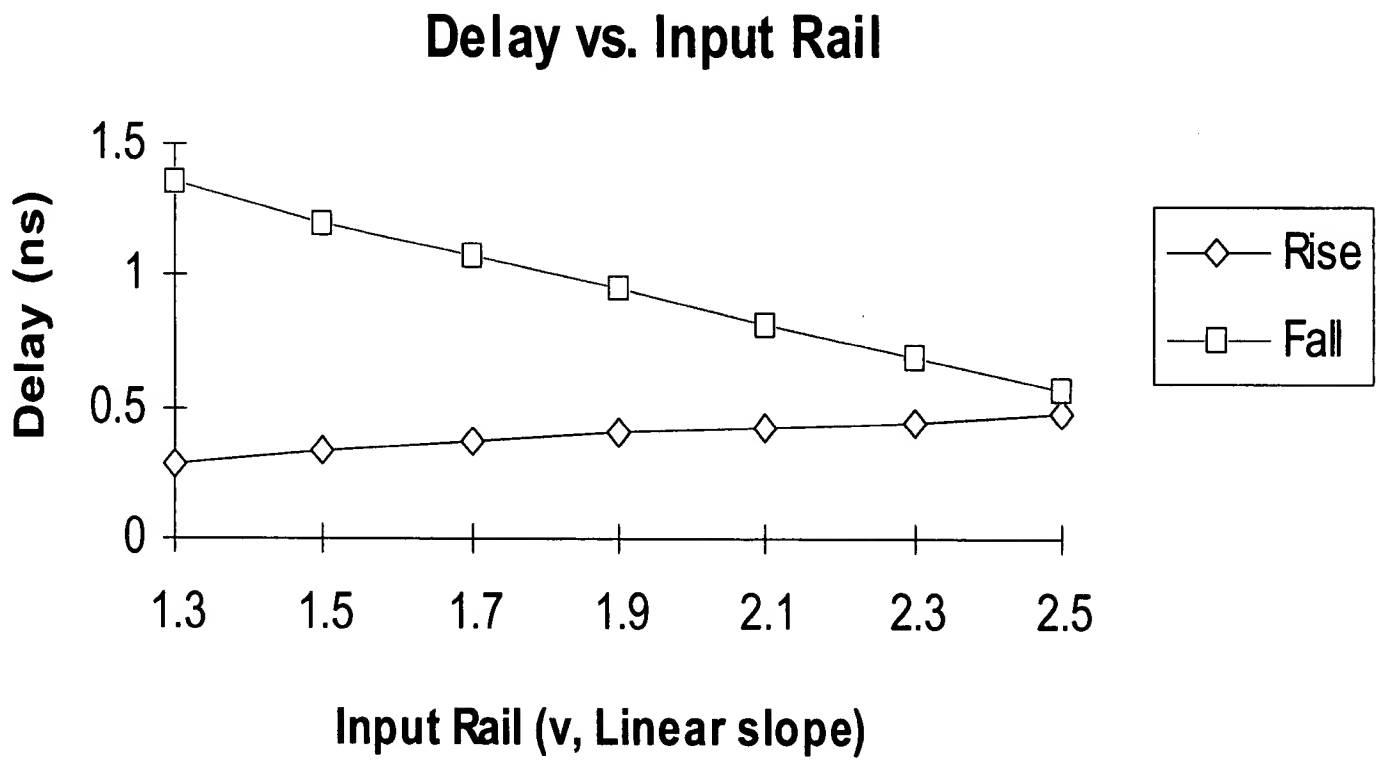
- @SSSS, -10C, 0.5pF
- Buffer doesn t switch at VCC < 1.4v, with 0.7v-1.7v linear input waveform.

Delay Characterization Data



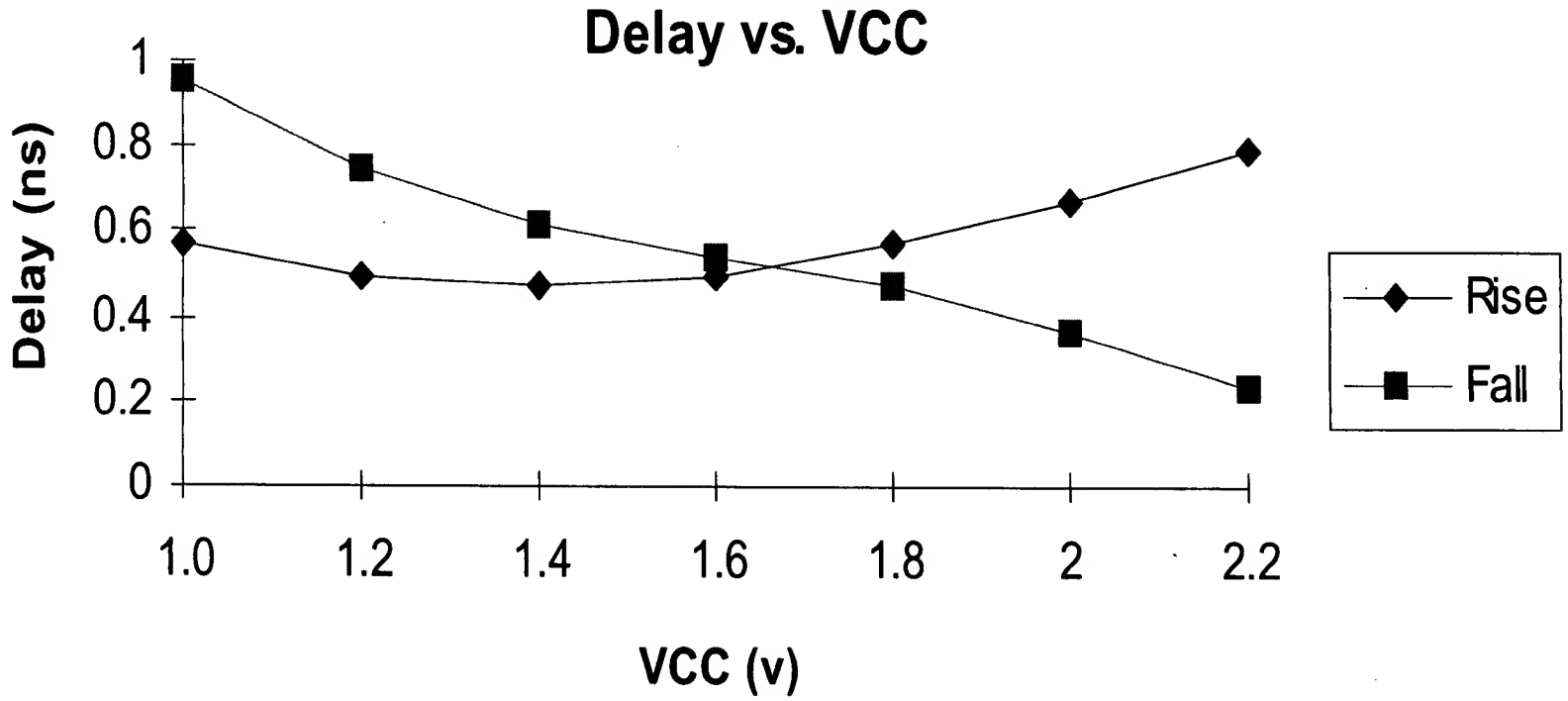
- @TTTT, 1.45v, 110C, 0.5pF

Delay Characterization Data



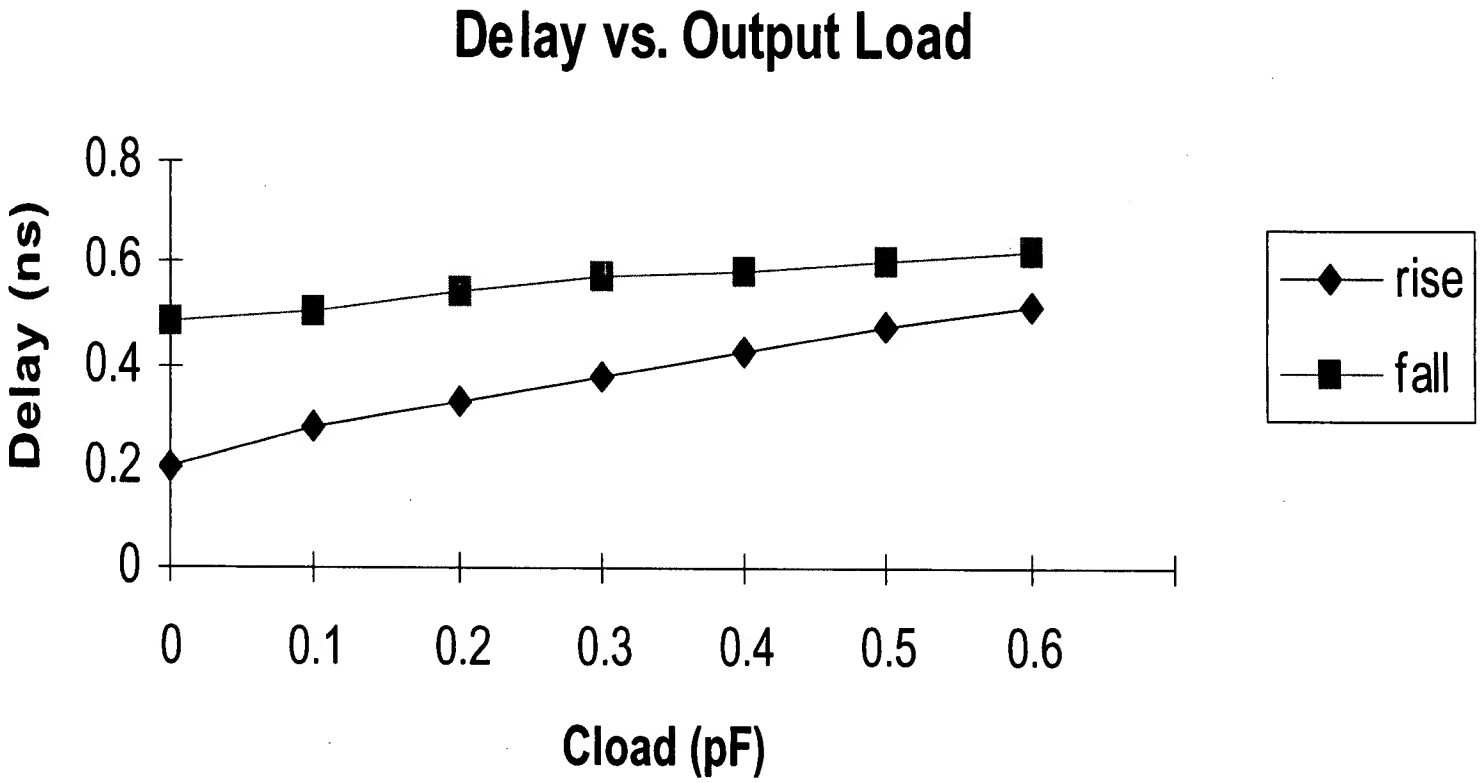
- @TTTT, 110C, 1.45v, 0.5pF
- Used linear input waveform.

Delay Characterization Data



- @TTTT, 110C, 0.5pF

Delay Characterization Data



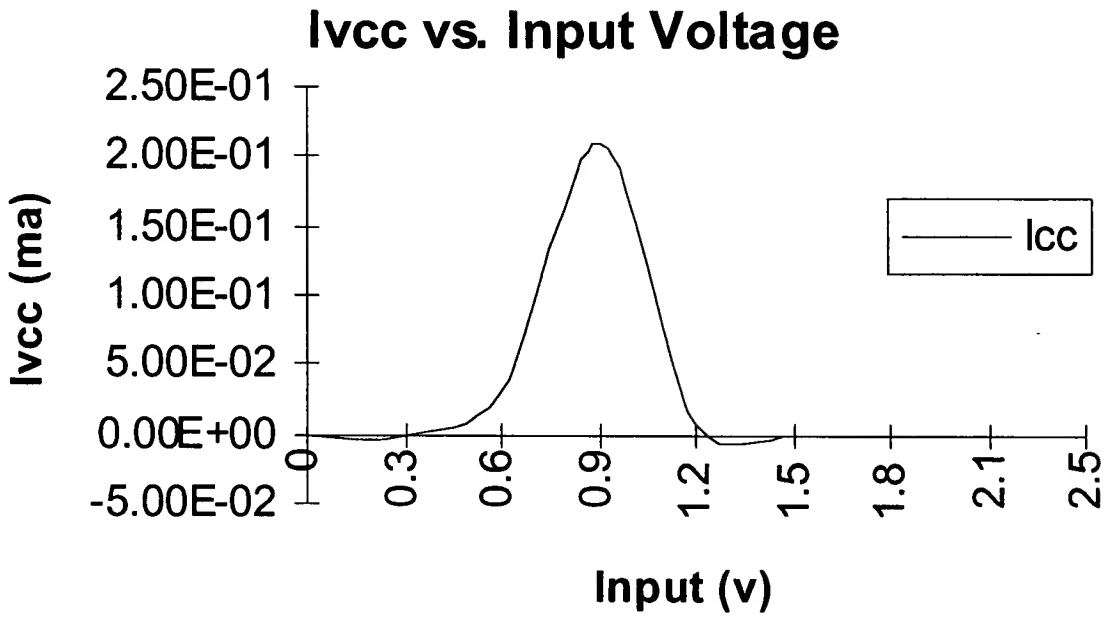
- @TTTT, 110C, 1.45v

Trip-Point Characterization Data

- SKEW VCC (V) TEMP. (C) TRI-POINT (V)

SKEW	VCC (V)	TEMP. (C)	TRI-POINT (V)
TTTT	1.8	50	1.07 (Typ)
TTTT	1.45	110	0.84
TTTT	2.05	-5	1.23
SSFS	2.2	110	1.41 (MAX)
FFSF	1.2	-5	0.62 (MIN)

Current Characterization Data



- @TTTT, 50C, 1.8v, 0.5pF
- Icc=1.7uA @ Vin=0.4v, Icc=11nA @ Vin=1.9v
- Icc=0.12mA @ TTTT, 50C, 1.8v, 0.5v/ns piecewise linear input.

Current Characterization Data

- **EM & SH Current Check:**

Pin	Size (W/L)	I_EM	I_SH
Padin		0.13mA	0.36mA
Vcc		14.6nA	0.13mA
i16	2/0.6	23.1nA	7.3uA
i19	15/0.48	0.21uA	37uA
i32	28/3	8.4nA	2.7uA
i5	0.6/2	0.83uA	2.5uA
i2	39/0.48	53.5uA	0.12mA
i18	3/0.48	53.6uA	0.11mA
i7	16/0.4	75.6uA	0.31mA
i20	25/0.4	73.7uA	0.42mA

- @TTTT, 1.8v, 110C, 0.5pF, 0.5v/ns input.

Delay Window

- ***P55C delay window: [0.21-1.34ns]***
- **0-2.5v piecewise linear input:**
  - 1v/ns slew rate:
    - MIN= - 0.12ns, @FFFF,1.2v,-5C,0.1pF
    - MAX=0.94ns, @SSSS,1.2v,-5C,0.1pF
  - 6v/ns slew rate:
    - MIN=0.17ns, @FFFF,1.2v,-5C,0.1pF
    - MAX=0.5ns, @SSSS,1.2v,95C,0.1pF

Delay Window continued

- **0.7v-1.7v linear input**:**
  - —1v/ns slew rate:
    - MIN=0.47ns, @FFFF,1.2v,-5C,0.1pF
    - MAX=4.92ns, @SSSS,1.2v,-5C,0.1pF
  - —6v/ns slew rate:
    - MIN=0.27ns, @FFFF,1.2v,-5C,0.1pF
    - MAX=3.77ns, @SSSS,1.2v,95C,0.1pF
- **The first inverter needs to be sized to Wp2/Wn2=420/3 for output to switch at VCC=1.2v, using this linear input waveform.

Architecture (MHPG/DE) (IA Comm)

Form: Intel Invention Disclosure, Rev 9, 9/96

LEGAL# 63584 P#_____
BSTZ# _____ SHSL#_____ DATE: FEB 20 1997

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to the Legal Department at JF3-147. If you have any questions regarding this form or to whom it should be forwarded, please call 264-0444.
PLEASE, PRINT CLEARLY OR TYPE.

1. Inventor(s):
Name: **Melik Isbara** SS# **136781700**
Empl. No. **10061341** Dept.# **7302-6** Phone **765-6457** M/S: **SC9-25**
Home Address: **1000 Escalon Avenue Apt. #J3076 Sunnyvale CA 94086**
Citizenship: **Turkish** Supervisor* **Sanjay Natu** Phone **765-6428** M/S: **SC9-25**
Group Name: **DE** Division Name: **MHPG** Subgroup Name: _____

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention:
AC coupled and bootstrapped voltage-tolerant input buffer for integrated circuits.

3. Stage of development, i.e. % complete, and relation of technology to the following product/process:
It has been designed and taped-out on P55C AQS. Si is currently being tested. It is also under consideration to be used on Tillamook. It, or an equivalent solution is required for mixed supply products where the peripheral voltage level is higher than the core voltage level.

4.(a) Has a description of your invention been, or will it shortly be, published outside Intel:
NO: X YES: ___ DATE WAS OR WILL BE PUBLISHED: _____ (fill in best estimate)
If YES, was the manuscript submitted for pre-publication approval?
YES: ___ NO: ___

(b) Has your invention been used/sold or planned to be used/sold by Intel or others?
NO: ___ YES: X DATE WAS OR WILL BE SOLD: _____ (fill in best estimate)

5. If invention conceived, or constructed during performance of a government or third party contract, please check here and give the contract name and number **n/a**.

6. Please attach a page to this form, DATED AND SIGNED BY ONE INVENTOR (PREPARER), to provide an abstract of your invention, and include the following information in your abstract:
(a) State general purpose(s) of your invention;
(b) Describe advantage(s) of your invention over what is done now;
(c) Describe essential element(s) or key to your invention; and
(d) Value of your invention to Intel (how will it be used?).

*HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM

DATE: 2/18/1997 SUPERVISOR: Sanjay Natu

RECEIVED
FEB 24 1997
S.T.Z. DATABASE DEPT.
R. Plaza

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

INTEL INVENTION DISCLOSURE
Intel Confidential

Title: AC coupled and bootstrapped voltage-tolerant input buffer for integrated circuits.

Purpose: Allow interfacing input signals with voltage levels above what is tolerable for gate oxides in a low-voltage IC process.

Advantages and value: This invention will simplify the input buffer design to interface bus signals with voltage levels higher than the core voltage in all low voltage Intel processes. Many products in these low-voltage processes will need to accept, or drive, signals at higher voltages to communicate with products operating at those voltages. The invention described herein combines CMOS pass-gate input buffer with an ac bypass capacitor to form a voltage divider in connection with the inverter's input capacitor. It does not require a resistive dc bias, thus providing a low power solution in a small area.

Description of essential elements: The simplest way to interface a bus voltage to lower core voltage is to drop the bus voltage to a safe level via a pass gate transistor (npg) as shown in Figure 1. After the pass gate, CMOS inverter sees Vbias-Vtn at its input until feedback PMOS device (plkr) pulls it to Vcc. One way to help to speed up the switching is to use bootstrapping by adding an active (plkr) or a passive resistor from Vbias to the gate of the pass-gate. This improves high to low transition while worsening low to high transition. Instead of solely relying on bootstrapping, having an ac bypass capacitor (pcap) across the pass transistor helps to improve the switching speed in low to high transition while not worsening it on high to low transition equally.

Value to Intel: This design is one of the input buffer evaluated on P55C AQS for Tillamook processor. It can provide a simple solution to interfacing to a higher bus voltage level in a small area. This in turn results in die-area and power savings.

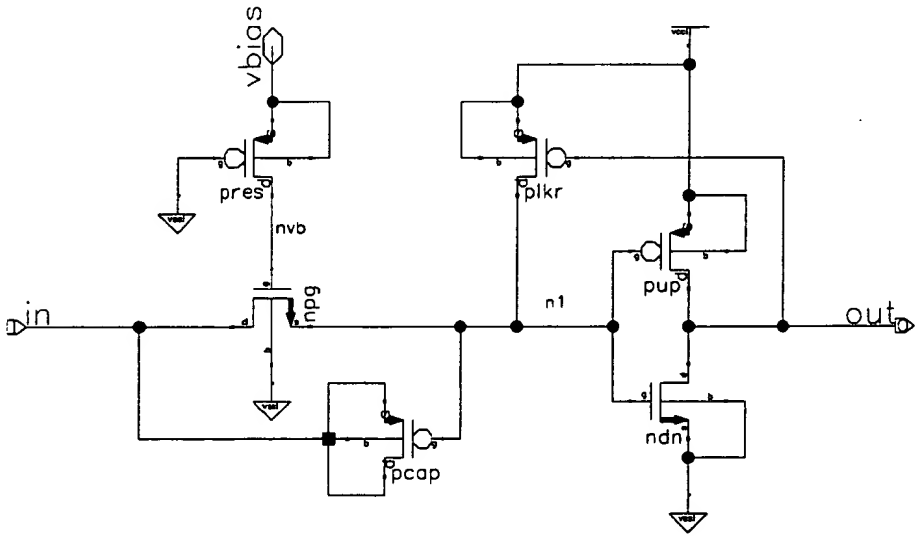


Figure 1. A simplified schematic of the buffer.

Name: Melik Isbara Date: 2/18/97 Signature: Melik Isbara

"Isbara, Melik" <melik.isbara@intel.com>
08/04/04 11:47 AM

To: <Farzad_Amini@bstz.com>
cc: "Isbara, Melik" <melik.isbara@intel.com>
Subject: RE: swearing behind a prior art reference

Farzad,

How does this sound to you?

Melik

Selection meeting minutes e-mail:
It states that using a broad set of evaluation criterias applied to the simulation results (very detailed simulations including layout extracted parasitics and the package models), input buffer named "inmis" overall performs better than the other candidates intended to be included in a test chip (named AQS) and a subsequent product. The other candidates were used on the previous products thus their simulation based performance were correlated to real measurements. The fact that inmis performed overall better than the other candidates using the same simulation assumptions/tools/techniques, it was expected that it's performance on the test chip or the product would be as good as simulations showed.

It is well established that simulations tools are very accurate and the results are closely correlated to real measurements within a few percentage.

----- Message from Unknown on Wed, 9 Oct 1996 18:25:11 -0700 -----

To: "/o=Intel/ou=Europa01/cn=Workers/cn=Stoler, Gil" <>,
"/o=Intel/ou=Americas01/cn=Workers/cn=Isbara, Melik" <>,
"/o=Intel/ou=Europa01/cn=Workers/cn=Wayner, Zelig" <>,
"/o=Intel/ou=Europa01/cn=Workers/cn=Gradstein, Amit" <>,
"/o=Intel/ou=Europa01/cn=Workers/cn=Yuffe, Marcelo" <>

Subject: I/O buffer selection meeting minutes

Attendees: Marcelo, Gil, Amit, Melik and Zelig.

In order to select the best input buffer for the Tillamook A step, before we analyze the AQS we decided to do a decision matrix:

Parameter	importance factor	inmis	ptc	ppc
Delay window	1.5	3/4.5	3/4.5	4/6
Sensitivity	1	5	5	3

to Vil				
Sensitivity to power fluctuations	1	5	4	5
Complexity	1	4	2	4
Rebustness	1	3	4	3
Flexibility	1	4	5	3
Total		25.5	24.5	24

Although accordingly to the decision matrix the best choice is the inmis input buffer Amit objected we should choose the ppc buffer due to its superior delay window.

Note the only two drawbacks of the ppc input buffer are its sensitibity to Vil and its lack of flexibility.

Amit decided he doesn't care of flexibility if he gets a better delay window. (ppc delay window is 0.5nS better than the inmis one).

It was also decided to take the Vil sensitivity risk as there are two factors that can reduce the risk: 1. it is likely the customers will approve the proposed Vil spec change. 2. the sensitivity can be better quantified in the AQS.

So it was decided to go for the ppc input buffer as first option and use the inmis input buffer as back-up.

In order to allow the fast change between input buffers it was decided to make the layout of ppc and inmis similar from an area and a port location point of view.

Since the ptc input buffer yields the minimum impact to the CLK DC skew, this input buffer will be still used for the CLK pin unless better analysis will show this buffer can be replaced by ppc (or inmis).

For the output buffers the decision was easier because we already have seen the delay window is the most important parameter and we are ready to take risk in order to get a better delay window.

A comparison between the different output buffer options brought us to the decision of using the NLSGSP output buffer (provided it is

approved by the QRE's). If this output buffer is not approved by the QRE's the AQSMOD2 output buffer will be used.

The most important differences between these two output buffers are:

	AQSMOD2	NLSGSP
Delay window	0.62 - 2.68	0.58 - 2.04
AQS tested?	Partially (AQSMOS is part of the AQS, however, AQSMOD2 implements minor changes).	yes
Gate stress?	No gate stress	2.7V gate stress for 0.6% of the lifetime
Active power	8.8mA	9.2mA
STPCLK power	20mW	0mW

Note the AC gate stress issue could veto the NLSGSP output buffer, in this case the AQSMOD2 output buffer will be used and therefore also here the layout should be done in such a way it will be easy to change between the buffers.